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(54) Method of manufacturing a gate electrode

(57) In an integrated circuit, gate electrode stack of which is subjected to self-alignment processes, the sheet resistance is lowered by including a tungsten layer 15. The tungsten layer 14 is protected by a sidewall material 21 of SiN_x or SiO_2 after an etching step which did not extend to the substrate 11. During a subsequent etching step in which the stack extends to the substrate 11, the sidewall material 31 acts as a hard mask protecting the upper portion of the stack. After the lower portion of the stack is protected by a re-oxidation layer 42, the entire stack can be processed further without deterioration of the sheet resistance of the tungsten layer 15.

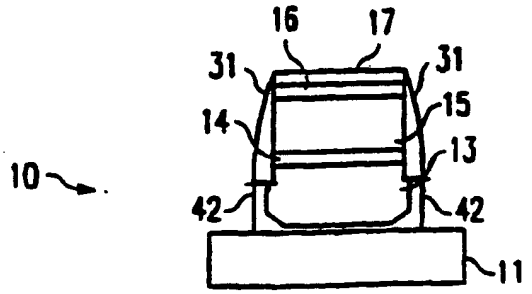

FIG. 4

EP 0 849 777 A2

Description

FIELD OF THE INVENTION

This invention relates generally to integrated circuits and, more particularly, to the fabrication of poly-silicon gate electrodes forming an integral part of selected integrated circuit components.

BACKGROUND OF THE INVENTION

In order to reduce the sheet resistance of a poly-silicon gate electrode, the use of a tungsten-capped poly-silicon stack has been proposed. However, to be compatible with the self-alignment contact process, the tungsten capped poly-silicon gate should have thermal stability up to approximately 900°C for 27 minutes in a nitrogen atmosphere without degradation of the sheet resistance and gate integrity; and have stability against oxidation up to approximately 800°C for 30 minutes in an air atmosphere.

A need has therefore been felt for process in which a tungsten layer can be incorporated into a poly-silicon gate electrode to reduce the resistance of the gate electrode while maintaining the desirable physical properties during the self alignment contact process procedures.

SUMMARY OF THE INVENTION

According to the present invention, provides an etching procedure which is stopped at the poly-silicon layer after etching a tungsten layer and a diffusion barrier layer. A protective layer of SiO_2 or a layer of SiN_x is then formed over the exposed surface. The layer of SiO_2 or SiN_x is etched in such a manner to provide a sidewall spacer on the exposed portions of the sides of the stack. The stack is then etched through a poly-silicon layer and a gate oxide (insulating) layer to the silicon substrate, with the previously etched portions of the stack and the sidewall spacer acting as hardmask for the further etching of the stack. A re-oxidation step reduces the etch damage to the gate oxide and reduces the leakage current at the bottom corner of the stack gate. The transistor stack, including the tungsten layer, retains the desirable physical characteristics after a processing operation which would, without the present procedures, have resulted in deterioration of these physical characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will now be further described by way of example, with reference to the accompanying drawings in which:

Figure 1 shows a gate structure after photoresist material has been applied to the gate structure and the photoresist material has been patterned;
Figure 2 shows a gate structure after removal of material not shadowed by the photoresist material, the photoresist material having been removed and a nitride coating applied;
Figure 3 shows a gate structure after a sidewall etch has removed a portion of the nitride coating; and
Figure 4 shows a gate structure after a re-oxidation step.

DETAILED DESCRIPTION OF THE DRAWINGS

Referring to Figure 1, the gate structure 10 is shown after the deposition and patterning of the photoresist material 18. The substrate 11 has a gate insulating (oxide) layer 12 formed thereon. Over the gate oxide layer 12 is formed a poly-silicon layer 13, the poly-silicon layer preferably being formed by low pressure chemical vapor deposition with a thickness of approximately 700-800 Angstroms. A diffusion barrier layer 14 of, for example titanium nitride, tungsten nitride, $Ti_xAl_{(1-x)}N_y$, or other materials (of approximately 50-200 Angstroms in thickness), which can block the inter-diffusion of tungsten and silicon, is formed on the poly-silicon layer 13 using either physical vapor deposition or chemical vapor deposition. A tungsten layer 15 of approximately 500-800 Angstroms is formed by either chemical vapor deposition or physical vapor deposition on the diffusion barrier layer 14. Over the tungsten layer 15 is formed a $Si_{(2x+1)}N_{(4x)}O_{(2-2X)}$ (where $x = 0 \rightarrow 1$) layer 16, and subsequently, an Si_xNi_4 (where $x \geq 3$) layer 17 is formed on the stack using a low pressure chemical vapor deposition (LPCVD) technique. The purpose of layer 16 is to protect the tungsten from oxidation during subsequent LPCVD deposition of SiN_x. Therefore, layer 16 is deposited at a temperature less than 400°C, (e.g., by plasma enhanced chemical vapor deposition with conventional plasma or electron cyclotron (ECR) plasma). Layer 16 is optional if the LPCVD Si_xN_4 (where $x \geq 3$) layer 17 is deposited in a deposition tool or chamber with the following conditions, (i.e., to prevent the tungsten from oxidation before the Si_xN_4 (where $x \geq 3$)

deposition):

(1) The wafers are loaded through an evacuated load-lock chamber into the deposition tube or chamber while the deposition tube or chamber is evacuated and maintained at an elevated temperature under; or

(2) The wafer is loaded into a deposition tube or chamber maintained at a low temperature (< 100°C). After evacuating the deposition tube or chamber, the wafer temperature is elevated to the desired temperature

A photoresist material layer 18 is deposited on the Si_xN_4 (where $x \geq 3$) layer 17 and patterned.

Referring to Fig. 2, the patterned photoresist layer 18 is used to control the stack etching. The stack is etched to stop substantially on or in the poly-silicon layer 13. After removing the remaining photoresist material and etch residues, a thin layer 21 of Si_3N_4 is formed over the exposed surface. Preferred deposition methods for this thin layer 21 of Si_3N_4 are the plasma enhanced chemical vapor deposition (with either an RF plasma or an electron cyclotron plasma) or a low pressure chemical vapor deposition with an evacuation step prior to deposition.

Referring to Fig. 3, the Si_3N_4 layer 21 is anisotropically etched to provide a sidewall spacer 31. The etch can be performed by a reactive ion etch or other anisotropic etch methods.

Referring to Fig. 4, the Si_3N_4 layer 21 is used as a hard mask for the etching of poly-silicon layer 13, stopping substantially on gate oxide layer 12. The whole stack 10 is processed with an oxidation step at 800±200°C to form an additional oxide region 42 at the edge of the poly-silicon layer and to repair damage to the gate oxide layer 12. The Si_3N_4 layer 21 has lower oxygen permeability, and thus will prevent tungsten from oxidizing during the 800±200°C oxidation step.

While the previous discussion has been devoted to a Si_3N_4 capping layer 21, a SiO_2 or $Si_{(2x+1)}N_{4x}O_{(2-2x)}$ (where x = 0->1) capping layer can similarly be used protect against the deterioration of the a stack tungsten layer.

Referring to Table 1, the effect of processing on the sheet resistance of the tungsten layer is shown. The stack being tested included a tungsten layer of approximately 800 Angstroms, a titanium nitride layer of approximately 100 Angstroms, a poly-silicon layer, a gate oxide layer, and a silicon layer. The preferred annealing process takes place for 20 minutes in an oxygen atmosphere at 850°C. As will be clear form Table 1, the

Table 1

Capping Layer	Initial Rs (ohms/square)	Final Rs (ohms/square)
SiO_2 (3k Angstroms)	2.34	1.96
Si_3N_4 (1k Angstroms)	2.34	1.66
Si_3N_4 (3k Angstroms)	2.34	1.65

resistivity of the tungsten layer is lowered during the processing operation. Therefore, the procedure described herein provides a viable technique for lowering the sheet resistance of a transistor stack by including a tungsten layer. The procedure includes process steps which protect the tungsten layer from deterioration during the self-alignment contract processing steps.

It will be understood by those skilled in the art that various changes may be made and equivalents substituted for elements of the illustrated embodiments without departing from the spirit and scope of the teachings disclosed herein. For example, the presence of the gate insulating layer and the diffusion barrier layer of the stack structure are not necessary to practice this technique. In the absence of these layers, the procedure for forming the sidewall regions would remain the same. The diffusion barrier layer, by way of specific example, is not necessary when additional processing does not involve temperatures above 550°C. Furthermore, although described with respect to a tungsten conducting layer, a molybdenum conducting layer can also be used to improve the conductivity of the poly-silicon layer. In addition, many modifications may be made to adapt a particular situation and material to the teachings disclosed herein.

As is evident from the foregoing discussion, certain aspects are not limited to the particular details of the examples illustrated, and it is therefore contemplated that other modifications and applications will occur to those skilled in the art.

Claims

1. A method for fabricating a gate stack for an integrated circuit comprising;

forming a gate insulating layer, a poly-silicon layer, a diffusion barrier layer, a conductive layer, an Si_xN_4 layer, and a patterned photoresist layer;

removing portions of at least said diffusion barrier layer, said conductive layer, and said Si_xN_4 layer, in regions where said photoresist layer is absent to form a first stack of layers;
forming a sidewall region adjacent said stack of layers;
removing portions of said poly-silicon layer adjacent said stack of layers such that said substrate is substantially exposed; and
re-oxidising exposed regions of said poly-silicon layer and said gate insulating layer.

2. The method as claimed in Claim 1, wherein said step of forming said conductive layer comprises forming a conductive layer from a material selected from a group of materials comprising: tungsten and molybdenum.

3. The method as claimed in Claim 1 or Claim 2, wherein said step of forming said Si_xN_4 layer comprises forming a Si_xN_4 layer in which $x \geq 3$.

4. The method as claimed in any preceding claim, wherein said step of forming said sidewall regions comprises forming a sidewall region from a material selected from a group of material comprising: Si_3N_4, SiO_2, and $Si_{(2x+1)}N_{4x}O_{(2-2x)}$.

5. The method as claimed in Claim 4, wherein said step of forming said sidewall region from $Si_{(2x+1)}N_{4x}O_{(2-2x)}$ layer comprises forming said sidewall spacer from $Si_{(2x+1)}N_{4x}O_{(2-2x)}$ in which $x = 1 \rightarrow 2$.

6. The method as claimed in Claim 4 or Claim 5, wherein said step of forming said sidewall regions comprises the steps of:

forming a layer of material selected from the group at least on exposed portions of said stack of layers;
etching said layer of material to form sidewall regions on said stack of layers.

7. The method as claimed in any preceding claim, wherein said step of forming said Si_xN_4 comprises the steps of:

forming a layer of Si_3N_4, SiO_2, and $Si_{(2x+1)}N_{4x}O_{(2-2x)}$ using a vapour deposition process;
forming a layer of Si_xN_4 using a low pressure chemical vapour deposition process.

8. A method of preventing oxidation of a diffusion barrier layer and a conductive layer in a stack of layers, which method comprising;
forming a sidewall layer over lateral regions of said diffusion barrier layer and said conductive layer.

9. The method as claimed in Claim 8 further comprising;
forming said conductive layer from a material selected from a group of materials comprising: tungsten and molybdenum.

10. The method as claimed in Claim 8 or Claim 9, wherein said step of forming said sidewall layer comprises forming said sidewall layer from a material selected from a group of materials comprising: Si_3N_4, SiO_2, and $Si_{(2x+1)}N_{4x}O_{(2-2x)}$.

11. The method as claimed in Claim 10, wherein said step of forming said sidewall layer from $Si_{(2x+1)}N_{4x}O_{(2-2x)}$ comprises forming said sidewall layer from $Si_{(2x+1)}N_{4x}O_{(2-2x)}$ in which $x = 0 \rightarrow 1$.

12. The method of any of Claims 8 to 11 further comprising;

forming said stack of layers from conductive layer, a diffusion barrier layer, a poly-silicon layer, and a gate oxide on a substrate; and
forming said sidewall layer such that it does not cover said poly-silicon layer and a gate oxide layer.

13. The method as claimed in Claim 12 further comprising the step of;
forming an oxide sidewall over said poly-silicon layer and said gate oxide layer.

14. A semiconductor stack comprising:

a gate oxide layer formed on a substrate;

a poly-silicon layer formed on said substrate, wherein said poly-silicon layer and said gate oxide layer have an oxide sidewall;
a diffusion barrier layer formed on said poly-silicon layer; and
a conducting layer formed on said diffusion barrier layer, wherein said diffusion barrier layer and said conducting layer have a sidewall barrier.

15. The stack as claimed in Claim 14, wherein said conducting layer is formed from a material selected from a group of materials comprising tungsten and molybdenum.

16. The stack as claimed in Claim 14 or Claim 15, wherein said sidewall barrier is formed from a material selected from a group of materials comprising S_iO_2 and SiN_x.

17. The stack as claimed in any of Claims 14 to 16, further comprising:
a SiN_X layer formed on said conducting layer.

18. The stack as claimed in any of Claims 14 to 17, wherein said sidewall barrier provides a hard mask for the etching stopping on or in a poly-silicon region and a gate oxide region to form said poly-silicon layer and said gate oxide layer.

19. A stack structure comprising:

a poly-silicon layer formed on a substrate;
a sidewall oxide formed on a wall of said poly-silicon layer;
a conducting layer formed on said poly-silicon layer; and
a sidewall layer formed on a wall of said conducting layer.

20. The structure as claimed in Claim 19, wherein said conducting layer is formed from a material selected from a group of materials comprising: tungsten and molybdenum.

21. The structure as claimed in Claim 19 or Claim 20, wherein said sidewall layer is formed from a material selected from a group of material comprising: SiN_X and Si0.

22. The structure as claimed in Claim 21, wherein said step of forming said SiN_X layer comprises forming an SiN_X layer in which X = 1 -> 2.

23. The structure as claimed in any of Claims 19 to 22, further comprising:
a gate insulating layer formed between said substrate and said poly-silicon layer, said oxide layer also formed on a wall of said gate insulating layer.

24. The structure as claimed in any of Claims 19 to 23, further comprising:
a diffusion barrier layer formed between said poly-silicon layer and said conducting layer, said sidewall material formed on a wall of said diffusion barrier layer.

25. A method for forming a conductive layer in an integrated circuit electrode gate stack, which method comprising:

forming on a substrate, a gate insulating layer, a poly-silicon layer, a diffusion barrier layer, a conducting layer, a Si_XN_4 layer, and a photoresist layer;
removing portions of said layers, where photoresist is absent at least to said poly-silicon layer, to form a first stack of layers;
forming a sidewall region of a material from a group of materials including Si_3N_4, $Si0_2$, and $Si_{(2X+1)}N_{4X}0_{(2-2X)}$;
removing material from said electrode gate stack to said substrate where said first stack and sidewall region are not present; and
re-oxidizing said exposed poly-silicon layer and said gate oxide layer.

26. A method of preventing oxidation of a diffusion barrier and a conducting layer in a semiconductor stack, said conducting layer selected from at least one of the group of materials consisting of tungsten and molybdenum, said method comprising the step of:
forming a sidewall material covering lateral areas of said diffusion layer and lateral areas of said conducting

layer, said sidewall material selected from a group consisting of Si02 and Si_3N_4 and $Si_{(2X+1)}N_{4X}O_{(2-2X)}$ (where X = 0 ->1).

27. A semiconductor stack formed on a substrate, said stack comprising:

a gate oxide layer formed on a substrate;
a poly-silicon layer formed on said substrate, wherein said poly-silicon layer and said gate oxide layer have an oxide sidewall;
a diffusion barrier layer formed on said poly-silicon layer; and
a conducting layer formed on said diffusion barrier layer, said conducting layer selected from at least one of the group of materials consisting of tungsten and molybdenum wherein said diffusion barrier layer and said conducting layer have a sidewall barrier.

28. A stack structure comprising:

a poly-silicon layer formed on a substrate;
a sidewall oxide formed on a wall of said poly-silicon layer;
a conducting layer on said poly-silicon layer; said conducting layer selected from at least one of the group of materials consisting of tungsten and molybdenum; and
a sidewall layer formed on a wall of said conducting layer, said sidewall material selected from a group of materials consisting of SiN_X and $Si0_2$ (where X = 1 -> 2).

29. A method for including a tungsten layer in an integrated circuit electrode gate stack, the method comprising the steps of:

forming on a substrate, in order, a poly-silicon layer, a conducting layer, a Si_XN_4 (X ->3) layer, and a photoresist layer, wherein said conducting layer is selected from at least one of a group of materials consisting of tungsten and molybdenum;
removing portions of said layers at least to said poly-silicon layer where a photoresist layer is not present to form a first stack of layers;
forming a sidewall region of a material selected from a group of materials including Si_3N_4, $Si0_2$, and $Si_{(2X+1)}N_{4X}O_{(2-2X)}$ (where X = 1 ->2);
removing material from said electrode gate stack to said substrate, where said first stack and sidewall region are not present; and
re-oxidizing said exposed poly-silicon layer and said gate oxide layer.

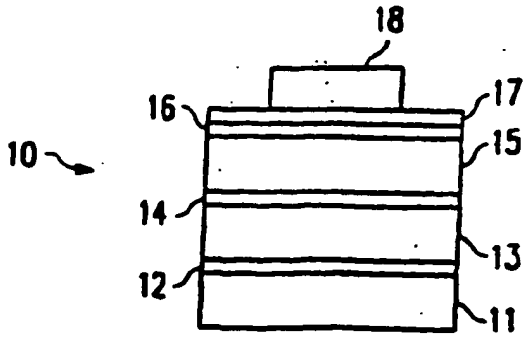

FIG. 1

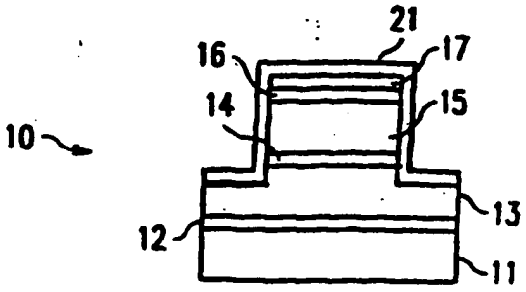

FIG. 2

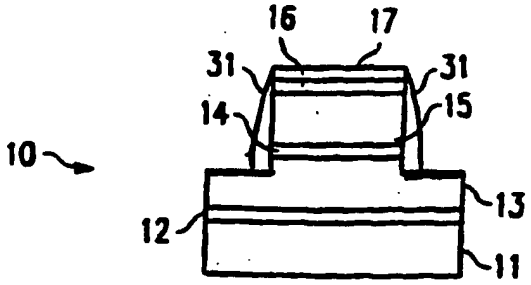

FIG. 3

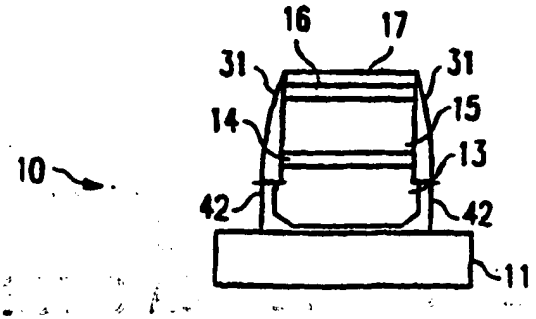

FIG. 4